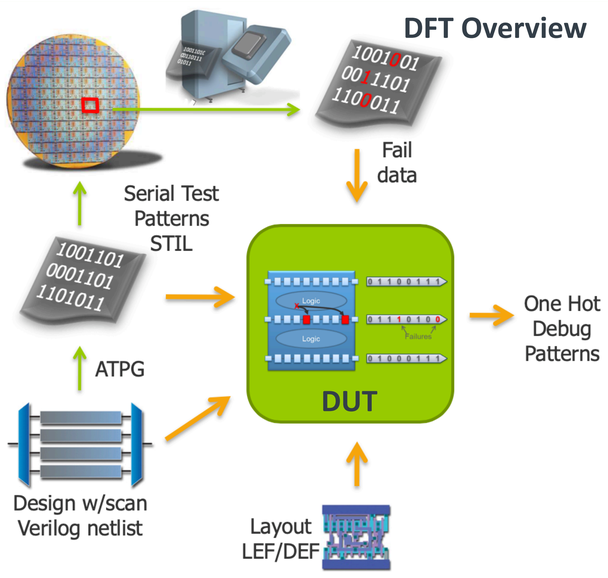
Accelerate Your Verification Using DFT Emulation

A real testchip showcasing reduction in verification time from weeks to minutes

Jitendra Aggarwal
Arm India

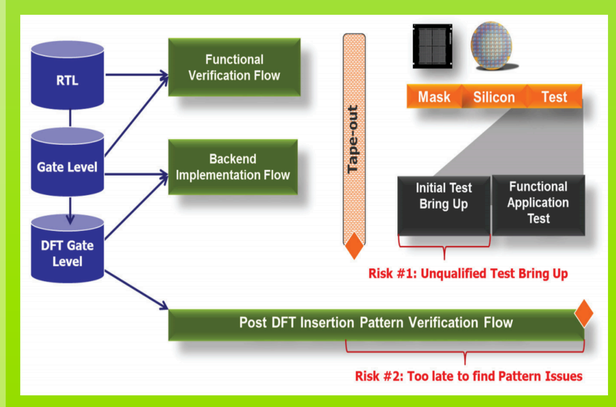
DFT Overview



DFT is a method to -

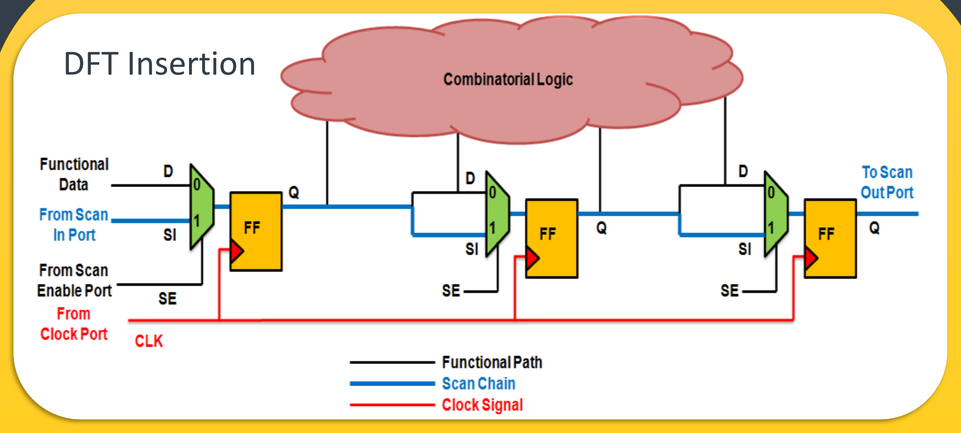
- Build testability into chips at the design stage to lower post-silicon testing costs
- Assure the detection of all faults in a circuit
- Reduce the cost/time associated with test development
- Reduce the execution time of fabricated chip testing

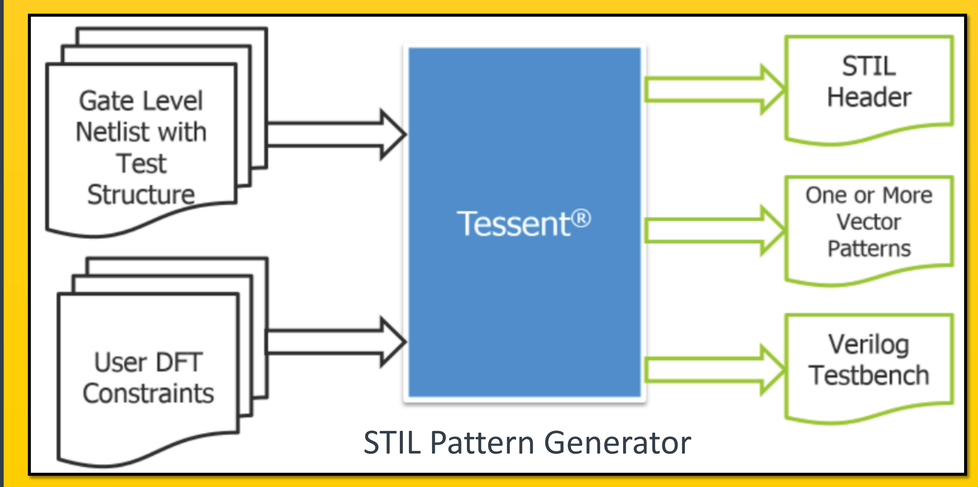
Simulation Drawbacks

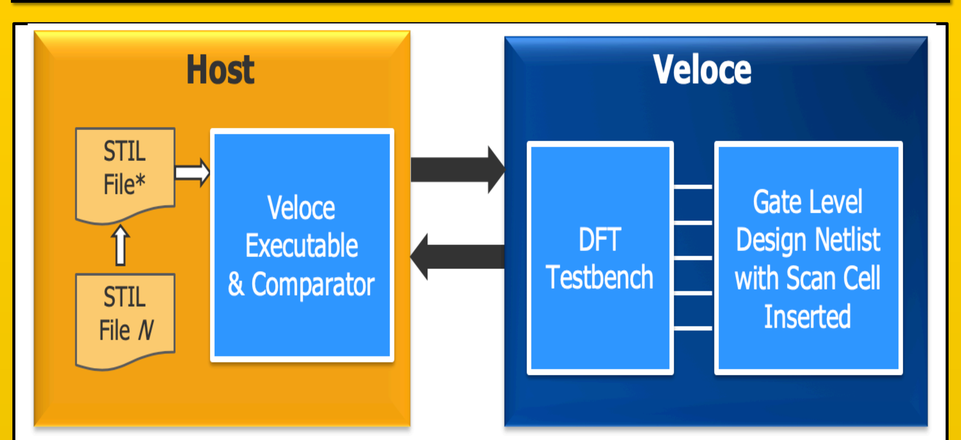


- Difficult to port large system-level designs
- Scan shift and pattern lengths increase complexity
- Less viable solution for a few test patterns

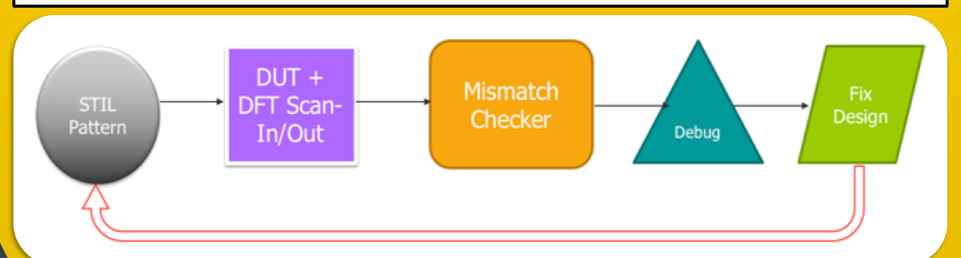
DFT Insertion



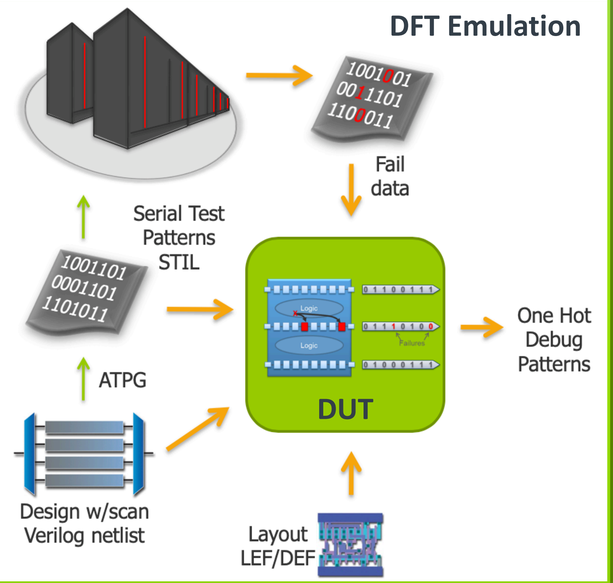




The Veloce DFT flow is fully automated with DFT transactors that read STIL files as input stimulus for patterns execution and comparison



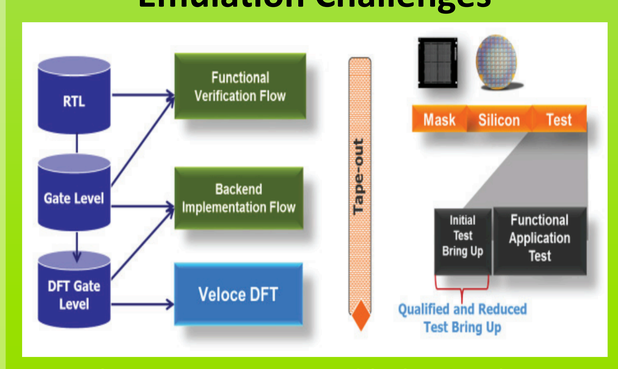
DFT Emulation



DFT emulation benefits -

- Seamlessly synthesize and port onto an emulator
- Every scan shift of any pattern length runs at MHz speed
- Faster DFT closure with simulation-like capabilities, including debug
- Reduces DFT effort from days to seconds

Emulation Challenges



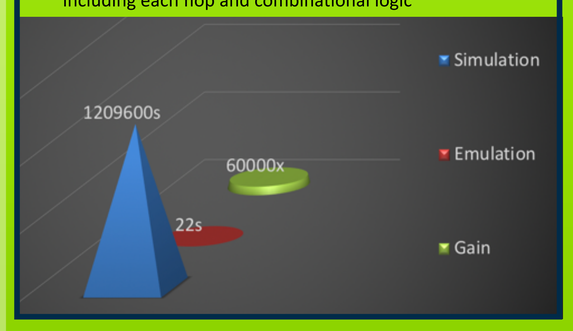
- Analog macros, PLL, and behavioral memories must be converted to synthesizable models
- Significant compile time due to synthesis and P&R steps involved in emulation
- Ring oscillator loops and long paths must be broken up manually

DFT Verification Timelines

DFT Verification Results

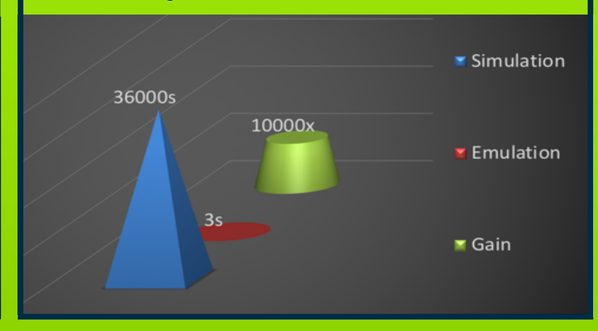
Serial Test-Pattern

- Highest performance gain in emulation
- Mainly used for sanity checks of DFT instrumentation logic
- Simulation is slower due to sequential exercise of stimulus
- One STIL pattern serially traverses from input to output, including each flop and combinational logic



Parallel Test-Pattern

- Access majorly state elements of design and provide stimulus directly to see behavior of fan-out logic
- Faster debug and higher performance gain in emulation
- Internal design node is accessible to narrow down to the exact bug



Conclusion

Some DFT patterns are not feasible to exercise on a simulator even with a month runtime; emulation yields faster turnaround times
DFT emulation overcomes all simulation challenges due to speed and debug ability; all patterns verified ahead of schedule

Future Work

Test scan dump networks using emulation to test scan interfaces to debug functional issues/bugs
Using emulation to exercise memory repair networks by fault injection and ensure correctness of repaired memory